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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/742,946	12/20/2000	Steven W. Rogers	5150-52100	8700

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EXAMINER	
KE, PENG	

ART UNIT	PAPER NUMBER
2174	7

DATE MAILED: 03/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/742,946	ROGERS ET AL.	
	Examiner	Art Unit	
	Peng Ke	2174	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 22 December 2003.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-40 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-40 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communications: Amendment, filed on 12/22/03. This action is final.

2. Claims 1-40 are pending in this application. Claims 1, 10, 18, 26, 32, and 39 are independent claims. In the Amendment, filed on 12/22/03, claims 1, 10, 18, 26, 32, and 39 were amended.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-40 rejected under 35 U.S.C. 102(e) as being anticipated by Yamamoto et al. (US 6,553,431).

As per claim 1, Yamamoto et al. teaches a method for propagating type information for hardware device nodes in a graphical program, wherein the method operates in a computer including a display screen and a user input device, the method comprising:

displaying on the screen a First hardware device node in the graphical program in response to user input wherein the graphical program comprises a plurality of interconnected

nodes or icons, wherein the plurality of interconnected nodes or icons visually indicate functionality of the program (Fig 6, col. 9 lines 7-19, Fig. 27A, items "A5F-1", "my digital camera", "engineer fax", "muto@cpdc");

associating the first hardware device node with a hardware device (Fig 9A, item 1, The Scan 5 note is associated with the input image scanner device) ;

displaying on the screen a second hardware device node in the graphical program in response to user input (Fig 9A, item 45, The reference displays a list of output device that suppose the input device);

connecting the first hardware device node to the second hardware device node in response to user input (Fig 9A, 9B, col. 10, lines 37-68, The connection between Scan 5 and LP5-1 is made, when the user place LP5-1 to a predetermined position.);

propagating information from the first hardware device node to the second hardware device node, wherein the information specifies the hardware device with which the first hardware device node is associated, wherein said propagating occurs in response to said connecting the first hardware device node to the second hardware device node (col. 3, lines 23-56).

As per claim 2, Yamamoto et al. teaches the method of claim 1, wherein said displaying the first and second hardware device nodes in the graphical program comprises including the first and second hardware device nodes in a block diagram of the graphical program, wherein the block diagram visually indicates functionality of the graphical program (Fig 9A. items 1, 2, 3).

As per claim 3, Yamamoto et al. teaches the method of claim 1, further comprising:

associating the second hardware device node with the hardware device with which the first hardware device node is associated, in response to said propagating the information to the second hardware device node (col. 3, lines 5-24).

As per claim 4, Yamamoto et al. teaches the method of claim 1, wherein said connecting the first hardware device node to the second hardware device node comprises connecting, a wire from an output terminal of the first hardware device node to an input terminal of the second hardware device node (col. 10, lines 59-66).

As per claim 5, Yamamoto et al. teaches the method of claim 1, wherein said associating the first hardware device node with a hardware device comprises associating the first hardware device node with a hardware device class corresponding to the hardware device (col. 9, lines 7-19);

wherein said propagating information from the first hardware device node to the second hardware device node comprises propagating information specifying the hardware device class with which the first hardware device node is associated (col. 3, lines 5-29).

As per claim 6, Yamamoto et al. teaches the method of claim 5, further comprising:

associating the second hardware device node with the hardware device class, in response to said propagating the information to the second hardware device node (col. 3, lines 5-29).

As per claim 7, Yamamoto et al. teaches the method of claim 6, further comprising:

associating the second hardware device node with a method of the hardware device class in response to user input (col. 3, lines 5-29; The list of the output devices is provided in response to the input device selected by the user.);

wherein during execution of the graphical program the second hardware device node is operable to invoke the method (col. 14, lines 25-43).

As per claim 8, Yamamoto et al. teaches the method of claim 6, further comprising:

associating the second hardware device node with a property of the hardware device class in response to user input(col. 10, lines 37-68) ;

wherein during execution of the graphical program the second hardware device node is operable to perform one or more of: 1) getting the property; and 2) setting the property (col. 12 lines 35-49).

As per claim 9, Yamamoto et al. teaches the method of claim 1, further comprising:

executing the graphical program, wherein during execution of the graphical program the second hardware device node is operable to access the hardware device (col. 12, lines 8-49).

As per claim 10, Yamamoto et al. teaches a method for performing type checking for a hardware device node in a graphical program, wherein the method operates in a computer including a display screen, the method comprising:

displaying on the screen a first hardware device node in the graphical program in response to user input (Fig 6, col. 9 lines 7-19);

associating the first hardware device node with a first hardware device class in response to user input (Fig 9A, item 1, The Scan 5 note is associated with the input devices);

selecting a method or property of the first hardware device class for the first hardware device node in response to user input;

changing the first hardware device node to have an association with a second hardware device class in response to user input (col. 9, lines 7-19); and

performing type checking to determine whether the method or property is valid for the second hardware device class, in response to said changing the first hardware device node to have an association with the second hardware device class (col. 10,lines 37-68, col. 11, lines 1-5).

As per claim 11, Yamamoto et al. teaches the method of claim 10, further comprising:

indicating an invalid condition if the method or property is not valid for the second hardware device class (col. 10, lines 65-68, col. 11, lines 1-5).

As per claim 12, Yamamoto et al. teaches the method of claim 11,

wherein said indicating the invalid condition comprises altering the visual appearance of a wire connected to an input terminal of the first hardware device node, wherein the wire provides information specifying the second hardware device class with which the first hardware device node is associated (Fig 9A, item A).

As per claim 13, Yamamoto et al. teaches the method of claim 10, further comprising: preventing execution of the graphical program if the method or property is not valid for the second hardware device class (col. 11, lines 6-11). It is inherent that if the selection is cancelled then execution of transferring path profile will be prevented.

As per claim 14, Yamamoto et al. teaches the method of claim 10, wherein the first hardware device node has an input terminal for receiving information specifying a hardware device class with which to associate the first hardware device node (col. 12, lines 35-49); It is inherent when the image is transferred to device, it is transferred into the input terminal of the device;

wherein said associating the first hardware device node with the first hardware device class comprises connecting a first wire to the input terminal (col. 11, lines 34-40);

wherein said changing the first hardware device node to have an association with a second hardware device class comprises connecting a second wire to the input terminal (col. 9, lines 30- 49).

As per claim 15, Yamamoto et al. teaches the method of claim 10, wherein the first hardware device node is a register access node (col. 3, lines 23-45). It is inherent that the hardwares that can be selected through the host computer are registered within the system.

As per claim 16, Yamamoto et al. teaches the method of claim 10, wherein said performing type checking to determine whether the method or property is valid for the second hardware device class comprises:

determining a list of valid methods and properties for the second hardware device class (col. 9, lines 50-54); and

determining whether the method or property is included in the list of valid method and properties (col. 9, lines 50-54).

As per claim 17, Yamamoto et al. teaches the method of claim 16, wherein said determining the list of valid methods and properties for the second hardware device class comprises determining the valid methods and properties from a type library, wherein the type library includes information regarding the second hardware device class (col. 9, lines 30-42). Examiner infers to file server as a type of library.

As per claim 18, it is rejected with same rationale as claim 1. (see rejection above)

As per claim 19, which is dependent on claim 18, it is of the same scope as claim 2. (see rejection above)

As per claim 20, which is dependent on claim 18, it is of the same scope as claim 3. (see rejection above)

As per claim 21, which is dependent on claim 18, it is of the same scope as claim 4. (see rejection above)

As per claim 22, which is dependent on claim 18, it is of the same scope as claim 5. (see rejection above)

As per claim 23, which is dependent on claim 22, it is of the same scope as claim 6. (see rejection above)

As per claim 26, it is rejected with the same rationale as claim 10. (see rejection above)

As per claim 24, which is dependent on clam 23, it is of the same scope as claim 7. (see rejection above)

As per claim 25, which is dependent on claim 23, it is of the same scope as claim 8. (see rejection above)

As per claim 27, which is dependent on claim 26, it is of the same scope as claim 11. (see rejection above)

As per claim 28, which is dependent on claim 26, it is of the same scope as claim 13. (see rejection above)

As per claim 29, which is dependent on claim 26, it is of the same scope as claim 14. (see rejection above)

As per claim 31, which is dependent on claim 26, it is of the same scope as claim 16. (see rejection above)

As per claim 30, which is dependent on claim 26, it is of the same scope as claim 15. (see rejection above)

As per claim 32, it is rejected with same rationale as claim 1. (see rejection above)

As per claim 33, which is dependent on claim 32, it is of the same scope as claim 2. (see rejection above)

As per claim 34, which is dependent on claim 32, it is of the same scope as claim 3. (see rejection above)

As per claim 35, which is dependent on claim 32, it is of the same scope as claim 5. (see rejection above)

As per claim 36, Yamamoto et al. teaches the system of claim 35, wherein the processor is further operable to execute program instructions stored in the memory to associate the second hardware device node with the hardware device class, in response to said propagating the information to the second hardware device node (col. 12, lines 8-34).

As per claim 37, which is dependent on claim 36, it is of the same scope as claim 7. (see rejection above)

As per claim 38, which is dependent on claim 36, it is of the same scope as claim 8. (see rejection above)

As per claim 39, it is rejected with same rationale as claim 10. (see rejection above)

As per claim 40, which is dependent on claim 39, it is of the same scope as claim 16. (see rejection above)

Response to Argument

Applicant's arguments filed on 12/22/03 have been fully considered but they are not persuasive.

Applicant's arguments focused on the following issues:

A) Yamamoto doesn't specifically teach or suggest hardware device nodes in a graphical program.

B) Yamamoto doesn't specifically teach or suggest hardware nodes within the same device.

Examiner disagrees:

A) Yamamoto teaches using graphical program nodes to represent printers (Fig. 9A). Printer is a hardware device, which is defined by Microsoft Computer Dictionary to be a physical component of a computer system, including any peripheral equipment such as printers, modems, and mouse devices.

B) Applicant doesn't not suggest in any way that first device node is within the same device as second device node in claim 1. Furthermore, the entire computer system, which includes inputs such: as scanner, mutocpdc, and engineer fax (Fig. 27A), and outputs such as: ipA5-2, DSA5-1 (Fig. 27B), is considered to be a single device.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peng Ke whose telephone number is (703) 305-7615. The examiner can normally be reached on M-Th and Alternate Fridays 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kristine L Kincaid can be reached on (703) 308-0640. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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